KENNETH J. COOL, P.C.

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TO: Cheryl Moore	FROM: Kenneth J. Cool – Reg. No. 40,570
COMPANY: Board of Appeals - USPTO	DATE: 7/23/2007
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PHONE NUMBER:	SENDER'S REFERENCE NUMBER: Docket No. 42390.P12943
RE: Appeal Brief	YOUR REFERENCE NUMBER: 10/027,978

☑ URGENT ☐ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ PLEASE RECYCLE

NOTES/COMMENTS:

Dear Ms. Moore,

This fax is being sent to you per your request to patent attorney Stuart Whittington. I am transmitting the following documents to you on Mr. Whittington's behalf:

1- Corrected p. 2 of Appellant's Brief (changes made shown in bold)

2- Appendix B (Evidence Appendix)

3- Appendix C (Related Proceedings Appendix)

Best regards,

/Kenneth J. Cool – Reg. No. 40,570/

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III. STATUS OF CLAIMS.

Claims 1-33 have at one time, been pending in the present application. Claims 1-13 and 29-33 were cancelled due to restriction and thus only claims 14-28 remain pending. Claims 14-28 stand finally rejected and are the claims subject to this appeal, which are reproduced in attached Appendix A.

IV. STATUS OF AMENDMENTS.

An after final amendment was submitted by Appellant on September 8, 2005 which only presented amendments to the Abstract to address certain objections. The Advisory Action dated November 1, 2005 indicated the amendment would be entered into the record.

V. SUMMARY OF CLAIMED SUBJECT MATTER.

Embodiments of the instant invention relate to microprocessor systems that use virtual memory addressing. One problem that may arise with systems that use conventional memory management unit (MMU) configurations is that the address translations and memory protection operations performed by MMUs may be time consuming relative to other operations of the system. (Specification, pg. 2, ll. 9-15). Most notably, in conventional MMU configurations, access to the physical memory and/or memory controller by an MMU may be constrained by a multiplexer or other interface and thus performing a table walk (a process of translating virtual address into physical memory addresses or visa versa) requires that requests from the MMU (and replies for the memory) travel through several levels of logic/flip-flops and often a clock domain.

APPENDIX B
(EvidenceAppendix)

There is no additional evidence relied upon in this Appeal.

APPENDIX C
(Related Proceedings Appendix)

There are no proceedings or decisions related to this Appeal.